Name, Lastname, Id #: 28.01.2014

Karadeniz Technical University
Faculty of Engineering
Dept. of Comp. Engineering
BİL 107 Resit Exam

1.a. Construct the truth table of the two's complement $Y_3Y_2Y_1Y_0$ corresponding to $X_3X_2X_1X_0$.

b. Design, but do NOT draw, simplified combinational logic circuit to compute two's complement of input by Karnaugh mapping.

2. From Wikipedia, the free encyclopedia:

A watchdog timer (WDT; sometimes called a Computer Operating Properly or COP timer, or simply a watchdog) is an electronic timer that is used to detect and recover from computer malfunctions. During normal operation, the computer regularly restarts the watchdog timer to prevent it from elapsing, or "timing out". If, due to a hardware fault or program error, the computer fails to restart the watchdog, the timer will elapse and generate a timeout signal. The timeout signal is used to initiate corrective action or actions. The corrective actions typically include placing the computer system in a safe state and restoring normal system operation.

a. Design a Watchdog timer to restart the computer which runs a mission critical operation. The computer outputs a quasiperiodic (almost but not quite periodic, from merriam-webster dictionary) signal in about 2.3 to 4.7 second intervals depending on the workload to reset the timer in order to avoid an unnecessary reset while running its mission critical task. The timer should generate a very short pulse to restart the computer, if the computer fails to reset the timer due to a bug in the program. Assume that there is 1 Hz periodic clock signal available and the computer system can be reset by a very short pulse applied to RESET input pin of the CPU.

b. Is there a simpler logic circuit (not a digital timer with clock input) to detect software failures indicated by the unacceptable delay of a expected quasiperiodic signal often called "Heart Beat" of the computer system? Explain briefly the theory of operation.