Microprocessors Spring 2021 Mid-term test

1. Performance of computers is limited not only by processor speed but also access time of memory which stores data to be processed. Semiconductor memory chip access time
a. is determined by the flip-flop response delay
b. is determined by gate delays in address decoders
c. is determined by both data and address bus buffers
d. is proportional to data bus width
e. none

2. What is the importance of Programmable Logic Array (PLA) in High Performance Computing
a. PLAs can replace many fixed function logic circuits to reduce chip count and cost
b. PLAs can be used as dedicated hardware to speed-up well known algorithms or tasks
c. PLAs can be programmed to speed-up any parallelizable algorithm by compiling programs to run on many PLAs in parallel
d. Even though PLAs are more expensive and have limited performance compared to Application Specific Integrated Circuits (ASIC), they are general purpose and programmable to run any algorithm
e. all

3. Which of the following building blocks should be used to construct a 32-bit processor unit with an ALU and shifter to process 16 registers.
a. 2 32-bit 16:1 multiplexer and one 4:16 decoder
b. 3 32-bit 16:1 multiplexer and two 4:16 decoder
c. 4 16-bit 32:1 multiplexer and one 5:32 decoder
d. 3 16-bit 32:1 multiplexer and two 5:32 decoder
e. none

4. Microprogrammed control is preffered in early microprocessor designs
a. because it executes instructions faster than hardwired control
b. because it is easier to design and users' performnce expectations was not high at that time
c. because manufacturers' opted for easy mitigation of design errors by microcode updates
d. because it is the only design method known at that time
e. none

5. Why is there a Control Data Register (CDR) and Control Address Register (CAR) in microprogrammed control even if it is possible to design without a CDR and a CAR
a. buffered bus designs are better even if they introduce delay
b. buffering improves fan out and suggested on shared bus designs
c. applying control signals of currently running microinstruction to processing unit and preparing next control signals by accessing control memory at the same time is possible which improves execution efficiency
d. CAR and CDR needs to be clocked by separate signals which reduces instructions executed per second
e. none

6. Hardwired control logic design
a. executes instructions very fast and also lets designers to correct design errors simply by microcode updates
b. is not easy for complex operations but executes very fast
c. executes instructions faster than one flip-flop per state

d. slower than one flip-flop per state since it needs an additional decoder
e. none

7. One flip-flop per state is a technique which simplifies hardware control logic design
a. but must be designed carefully to initialize the control logic in the first state
b. and uses less number of flip-flops compared to sequence register and decoder
c. and uses less number of transistors since it does not need an additional decoder
d. generates control signals slower than a sequence register and decoder due to its asynchronous nature
e. none

8. How many memory references does an Assembly language program make to evaluate A-(B+C) and store it at address X
a. 6 b. 7 c. 8 d. 9 e. 10

9. The number of hardware control signals of a microprocessor is
a. proportional to the number of instructions
b. proportional to the produ?t of number of instructions anc addressing modes
c. depends on the number of unique number of microinstructions
d. not related to microprocessor instruction set
e. none

10. How many instructions does an assembly language program of a single accumulator organization microprocessor needs to multiply a signed binary number at address X by -1 and store the product to X
a. 1 b. 2 c. 3 d. 4 e. None

ANSWERS

1 B, 2 E, 3 A, 4 B, 5 C, 6 B, 7 A, 8 E, 9 C, 10 D