Karadeniz Technical University
Faculty of Engineering
Department of Computer Engineering
COM 204 1st Midterm Exam

1. A digital system has 3 registers AR, BR and QR. Three flip-flops provide the control variables of the system: S is a flip-flop set by an external start signal to start the system operation; F and R are two flip-flops used for sequencing the micro-operations when the system is in operation. A fourth flip-flop D is set by the system when the operation is completed. List the register transfer operations to integer divide AR by BR (by repeated subtraction) and compute the quotient in register QR.

$$S: QR \leftarrow \emptyset, S \leftarrow \emptyset, D \leftarrow \emptyset, F \leftarrow 1$$
$$F: F \leftarrow \emptyset, \text{ if } (AR < \emptyset) \text{ then } D \leftarrow 1 \text{ else } R \leftarrow 1$$
$$R: QR \leftarrow QR + 1, AR \leftarrow AR - BR, R \leftarrow \emptyset, F \leftarrow 1$$

2. List the sequence of micro-operations to add the accumulator to the memory addressed by the operand following the instruction code. In other words, the instruction should perform the operation M[ADRS] ← M[ADRS] + AC

$$DR \leftarrow M[PC]$$
$$IR \leftarrow DR$$
$$PC \leftarrow PC + 1$$
$$DR \leftarrow M[PC]$$
$$AR \leftarrow DR$$
$$PC \leftarrow PC + 1$$
$$DR \leftarrow M[AR]$$
$$AC \leftarrow AC + DR$$
$$DR \leftarrow AC$$
$$M[AR] \leftarrow DR$$
$$TC \leftarrow \emptyset$$

3. Frequency of a digital signal is related to the number of level transitions during an interval. Derive an algorithm in **flowchart** form to count transitions of the input signal stored in register R0. Register R1 is used to count transitions and word length of R0 is stored in R2. For example, there are 7 transitions in 01010101 and 1 transition in 00001111.

$$R1 \leftarrow \emptyset$$

$$R2 \leftarrow R2 - 1$$

$$C \leftarrow shr \ R\emptyset$$

$$C : ? \quad 0 \quad 1$$

(A) (B)

$$R2 \leftarrow R2 - 1 \qquad R2 \leftarrow R2 - 1$$

$$\neq \emptyset \quad R2 : \emptyset \quad = \emptyset \qquad = \emptyset \quad R2 : \emptyset \quad \neq \emptyset$$

$$C \leftarrow shr \ R\emptyset \qquad SON \qquad C \leftarrow shr R\emptyset$$

$$\emptyset \quad C : ? \quad 1 \qquad \emptyset \quad C : ? \quad 1$$

$$R1 \leftarrow R1 + 1 \qquad R1 \leftarrow R1 + 1$$

(B) (A)