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Karadeniz Technical University

Faculty of Engineering

Department of Computer Engineering

COM 204 2nd Midterm Exam

1. Write an assembly language program to add two IEEE-754 single precision unsigned numbers stored at addresses OPERAND1 and OPERAND2 and store the sum into SUM using the **L**oa**D** **A**ccumulator (LDA), **ST**ore **A**ccumulator (STA), **AD**d with **C**arry (ADC) and **CL**ear **C**arry (CLC) instructions of a single accumulator 8-bit microprocessor.

```
CLC                 /* Clear the CARRY flag before addition
LDA   OPERAND1      /* Load the Least Significant Byte (LSB) of the 1st operand
ADC   OPERAND2      /* Add with Carry the LSB of the 2nd operand
STA   SUM           /* Store the LSB of sum
LDA   OPERAND1+1    /* Load second Byte of the 1st operand
ADC   OPERAND2+1    /* Add second Byte of the 2nd operand
STA   SUM+1         /* Store second Byte of the sum
LDA   OPERAND1+2    /* Load third Byte of the 1st operand
ADC   OPERAND2+2    /* Add third Byte of the 2nd operand
STA   SUM+2         /* Store third Byte of the sum
LDA   OPERAND1+3    /* Load Most Significant Byte (MSB) of the 1st operand
ADC   OPERAND2+3    /* Add MSB of the 2nd operand
STA   SUM+3         /* Store MSB of the sum
```

2. The data transfer rate of peripherals is usually slower than that of microprocessors. Propose
a. a hardware and

A dual port buffer or a First In First Out type of memory should be used in order not to slow down a fast processor interfacing with a slow peripheral. Hardware FIFO's are made up of a dual port memory addressed by two ring counters allowing simultaneous read and writes. Thus a fast microprocessor fills the FIFO very fast and resumes computation whereas the peripheral reads FIFO slowly. Read operations decrement the number of bytes stored in the FIFO and if it drops below a Low Level Threshold, the FIFO interrupts processor to fill it up again before an Under Run.

b. a software to successfully interface the two dissimilar units without slowing down the microprocessor and explain their operation?
Hint : An optical drive of a computer system can be considered as a slow peripheral.

A software buffer or a FIFO can be used instead of a hardware buffer or they can be used together for much better performance. A software buffer is a block of main memory addressed by two pointers one for read and the other for write operations. A software FIFO emulate a hardware FIFO but makes use of memory to reduce cost. It is slower than a hardware FIFO but faster than a slow peripheral.

3. Explain the problem arising from unexpected termination (not receiving) of handshaking signals. Propose a mechanism to overcome the problem and handle synchronization of peripherals to communicate by handshaking signals and describe its operation.

   Unexpected termination of handshaking signals may cause the receiver to wait a valid signal from the sender forever. Time out mechanism can be used by the receivers which terminate the wait and start the synchronization process again.

4. The frame boundaries of bit-oriented protocols are determined from a special 8-bit number called a flag or **F**rame **S**ync **S**equence. Propose a method to ensure that a FSS pattern never appear in the payload (data) part of frames and describe its operation?

   FSS is an 8-bit sequence of 01111110 and could terminate a bit-oriented protocol if it appears in the payload. Except FSS, the transmitter should insert a 0 bit (zero insertion) after 5 consecutive 1 bits to make sure that the bit pattern does not resemble a FSS pattern in the payload. The receiver should remove extra 0 bit after 5 consecutive 1s in order to recover the original bit pattern.